

## ECPE Tutorial in the frame of EPE-ECCE 2016 Conference in Karlsruhe

### 1) Title of Tutorial

#### **Power Circuits for Clean Switching and Low Losses**

### 2) Abstract

This tutorial will teach the various effects of parasitic inductance ( $L_s$ ) in power electronics. As power density and current density is continuously rising, parasitic inductance and resistance become more and more the limiting factors. The problem is the product inductance times current ( $L_s \cdot I$ ) rising, simultaneously, if designs do not improve.

Not only overvoltage during switching is the problem but for bipolar power semiconductors like IGBTs and freewheeling diodes, parasitic inductance causes disadvantageous current waveforms.

In systems which have snubber capacitors additional to the DC-link capacitor and parasitic inductance in between, oscillations between these capacitors occur.

When considering power semiconductors in parallel the current sharing of controlled devices like IGBT, MOSFET and JFET can be affected by the presence of small parasitic inductance.

Parasitic inductance in the control circuit (gate circuit) decouples driver and the gates of the devices leading to increased short circuit current, for example.

To introduce these topics the tutorial will start with the basics of switching inductive loads and discussion of related waveforms. Investigations on the different effects will follow. The discussion of paralleling will be accompanied by case studies. Geometries of conductors and system design for low parasitic inductance and good current sharing will be another main part and the conclusions will summarize the benefits of related system design – clean switching and low losses.

### 3) Topical Outline and Schedule

09:30 - 11:00 Part 1:

- Power Semiconductors Switching under Inductive Load
- Geometry of Conductors and their Inductance – Determination and Evaluation
- Parasitic Inductance – Effecting Switching Characteristics and Stress Factors of Power Semiconductors

11:00 - 11:30 Coffee break

11.30 - 13:00 Part 2:

- Power Devices Parasitic Inductance – Effecting Current Sharing of Paralleled Power Devices
- Parasitic Inductance – Effecting System Losses
- Oscillations in DC-Bus

13:00 – 14:00 Lunchtime

14:00 - 15:30 Part 3

- Parasitic Inductance meets Parasitic Resistance
- Gate Inductance

15:30 - 16:00 Coffee break

16:00 - 17:30 Part 4

- Measuring Challenges and Solutions
- Benefit of Circuits with Low Parasitic Inductance

#### 4) Instructor

Dr. Reinhold Bayerer, Infineon Technologies AG, Germany

#### 5) Instructor's Biography



Reinhold Bayerer studied physics at the Technical University of Darmstadt, Germany and completed in 1979. He continued at this University as Research Associate and achieved his doctor's degree in physics in 1985.

He works in the field of IGBT Modules since then. A first paper on early IGBT-modules was given at PCI, Munich, 1987. He contributed to the fields of packaging technology, low inductance module design, test and application engineering, driver electronics, as well as manufacturing engineering. Several publications and patents may serve as a reference. Today, he is Fellow for physics of power modules and working at Infineon Technologies in Warstein, Germany.